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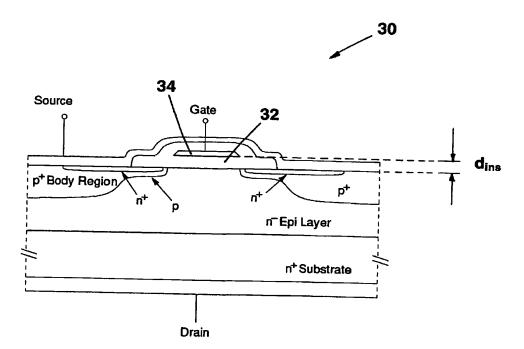
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[Continued on next page]

(54) Title: FAST SWITCHING POWER INSULATED GATE SEMICONDUCTOR DEVICE



(57) Abstract: An insulated gate semiconductor device (30) includes a gate (34), a source terminal, a drain terminal and a variable input capacitance at the gate. A ratio between the input capacitance (C_{fiss}) when the device is on and the input capacitance C_{iiss} when the device is off is less than two and preferably substantially equal to one. This is achieved in one embodiment of the invention by an insulation layer (32) at the gate having an effective thickness d_{ins} than a minimum thickness.



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H03K17/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

 $\label{eq:minimum} \begin{array}{ll} \mbox{Minimum documentation searched} & \mbox{(classification system followed by classification symbols)} \\ \mbox{IPC 7} & \mbox{H01L} & \mbox{H03K} \end{array}$

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ, INSPEC, WPI Data

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8 July 2004	22/07/2004				
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2	Authorized officer				
NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Lantier, R				

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